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10/812,020	03/30/2004	Kang-seok Cho	1572.1312	2784

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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,020	CHO, KANG-SEOK	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1, 2, 4, and 6-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-8, 11, 12, 14, 15, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki, U.S. Patent No. 6,446,213 B1, in view of Watts, U.S. Patent No. 6,336,161 B1.

Regarding claim 1, Yamaki teaches:

a system memory [Fig. 2, system memory 13];

a power management controller to control a supply power to the system [power supply controller 16];

and a controller to enable a power saving standby mode [EC 18], to control the power management controller to store an operating state stored in the system memory when the power saving standby mode is selected [col. 10, lines 37-47].

In comparison to claim 1, although Yamaki teaches that the embedded controller [EC 18] enables a power saving standby mode [sleep, col. 10, lines 41-43] and stores an operating state in the system memory when the power saving mode is selected [col. 10, lines 43-45, col. 11, lines 46-48], Yamaki does not specifically teach that the operating state is saved to flash

memory. The examiner notes that Yamaki does teach that the main memory maintains a self-refresh state, wherein "the main memory will maintain by itself" [col. 11, lines 42-45]. Although Yamaki is silent as to how the main memory maintains self-refresh, it is conceded that the main memory must be supplied some amount of power from the system in order to maintain the self-refresh state.

Watts teaches a system that saves its operating state to a flash EEPROM prior to entering a power off state [Watts, Fig. 3a, col. 2, lines 34-37].

It would have been obvious to one of ordinary skill in the art to modify the invention of Yamaki by saving the operating state to a flash EEPROM before entering a power off state, as taught by Watts. Both Yamaki and Watts are directed towards techniques for placing a computer into a power off mode, wherein the operating state of the computer is saved to a memory prior to removing power. However, as pointed out previously, the main memory of Yamaki is a dynamic memory that maintain a self-refresh state, and thus requires power to maintain its contents. Watts teaches that the most effective technique for conserving energy in a computer system is to completely remove power [col. 1, lines 20-22]. However, Watts concedes that completely removing power from prior art computer systems is not practical because restarting the computer is time consuming and does not allow the computer to be restored to the state prior to removing power [col. 1, lines 22-31]. Thus, Watts teaches an improvement upon the prior art wherein the operating state is stored in a flash EEPROM prior to completely shutting down power. In addition to the benefit of being able to restore a previous operating state quickly, the flash EEPROM provides an improvement in power savings over the prior art systems because the flash EEPROM requires no power to maintain its contents [col. 3, lines 57-58], thus allowing the computer system to realize a maximum of power saving by removing all power from the system, as suggested by Watts in col. 1, lines 20-22. Therefore,

the flash EEPROM of Watts would improve the system of Yamaki by obviating the need for a self-refreshing memory, and thus realizing improved power saving by obviating the need to provide power to maintain the self-refresh memory. The teachings of Watts regarding the improvements represented by the flash EEPROM and the desirability to completely remove power from a computer system for maximum power savings would have provided sufficient motivation to one ordinary skill in the art to combine the two inventions.

Independent claims 14 and 20 are rejected for reasons similar to claim 1. Regarding claim 20, Yamaki teaches that the storing of the operating state is performed in a BIOS [col. 11, lines 46-51].

Regarding independent claims 6 and 18, Yamaki and Watts teaches the computer system of claims 1, 14, and 20. Yamaki and Watts also teaches the method that is implemented by the claimed computer system.

Regarding claim 4, Watts teaches that the controller stores the operating state stored in the flash memory to the system memory when the power saving standby mode is changed to a normal mode in which normal operations are conducted [Fig. 3b, steps 64, 66]. Yamaki also teaches that the HW context is restored upon resuming a normal mode [Fig. 8, step S460, also col. 10, lines 50-53].

Regarding claim 7, Watts teaches re-supplying power to the system when the power saving standby mode is changed to a normal mode in which normal operations are conducted and storing the operating state stored in the flash memory to the system memory [Fig. 3b].

Regarding claim 8, Watts teaches that the power saving standby mode is selected via a user interface [col. 4, lines 10-12].

Regarding claims 11 and 15, it would have been obvious to one of ordinary skill in the art to provide a power management setup window in which the power saving standby mode is

enabled. Watts teaches that the power saving standby mode may be user enabled [col. 4, lines 10-12], and that the Windows NT operating system is in view [col. 4, lines 53-57]. Additionally, at the time of the invention of Watts, the Windows operating systems were well-known in the art.

Regarding claim 12, Watts teaches that a predetermined time is set to enter the power saving standby mode [col. 4, lines 10-13].

Regarding claim 17, Yamaki teaches that the storing of the operating state is performed in a BIOS [col. 11, lines 46-51].

Regarding claim 18, Yamaki/Watts teaches a method with steps comprising [Watts Fig 3a, 3b]:

copying an operating state date stored in the system memory to a flash memory when a power saving standby mode of the computer system is activated; and

copying the operating state data back to the system memory when a normal mode of the computer system is activated.

Additionally, Yamaki teaches a power management controller to control a power supply [power supply controller 16].

Regarding claim 19, Watts teaches that the normal mode of the computer system is activated without a booting process [col. 2, lines 41-45].

Claims 2, 9, 10, 13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki in view of Watts as applied to claims 1, 6-8, 11, 12, 14, 15, and 17-20 above, and further in view of Park, U.S. Patent Application Publication No. 2003/0145191 A1.

Regarding claim 2, although Yamaki/Watts teaches the computer system of claim 1, Yamaki/Watts does not teach that the flash memory is connected to the computer by a USB port.

Park teaches a detachable flash memory device that may be used to store the operating state of a computer system as it enters a power saving mode [paragraph 12, Fig. 3]. Park also teaches that the detachable flash memory is comprised of a USB device [paragraph 39].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Park with that of Yamaki/Watts by further modifying the flash EEPROM of Yamaki/Watts as a detachable USB flash device, as taught by Park. Yamaki, Watts, and Park are all directed towards techniques for saving an operating state of a computer system as it enters a power saving mode. While continuing to provide the benefits of retaining a previous operating state and maximizing power savings by completely removing power, the addition of Park's teachings would further improve the combination of Yamaki/Watts by enabling the user's operating environment to be transferred to other computers. This allows the user greater flexibility to work in different locations without having to adapt the computer to the desired operating state [Park, paragraphs 3, 5, 6, and 9].

Regarding claim 9, Park teaches selecting a standby mode or maximum power saving mode, checking whether the flash memory is connected to the system, and determining the selection when the flash memory is connected [Fig. 3, steps 34, 36, 38, paragraph 28 and 29].

Regarding claims 10, 13, and 16, Park teaches a USB flash device [paragraph 39]; therefore the device is detachably provided to the computer system, and the USB port is used to restore/save from/to the flash memory device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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